REMARKS/ARGUMENTS

According to the Office Action, claims 1-4, 6-10, 13-20, 22-29, and 31-34 stand rejected under 35 U.S.C. 103(a) for allegedly being unpatentable over U.S. Patent 6,591,091 (Vorenkamp et al.) in view of U.S. Patent 6,172,579 (Dacus et al.). Claims 5, 21, and 30 stand rejected under 35 U.S.C. 103(a) for allegedly being unpatentable over the Vorenkamp Patent in view of the Dacus Patent, and further in view of U.S. Patent 5,953,645 (Grondahl).

In response, claims 2, 3, 18, 19, 27 and 28 are cancelled. Independent claims 1, 4, 9, 17, 20, 26, and 29 are amended to further recite the following elements:

> a first amplification stage having a relatively high gain to cause saturation of said first amplification stage; and
>
> a second amplification stage comprising a linear power amplification stage that is current limited to lower the compression point to enhance a rise time and harmonic content of said substantially square wave signal

Such elements are neither described nor suggested in the cited prior art references. Furthermore, the main cited reference Vorenkamp teaches away from using multiple amplification stages, let alone a specific arrangement of multiple amplification stages as claimed:

> In the prior art, signal transformation from a sinusoidal signal to a square wave output is typically implemented by using an inverter to square sinusoidal input signal. A digital inverter function might be characterized as a nonlinear amplifier of a transformed sinusoidal input signal to a square wave by providing extremely high gain, such that the input signal is driven to the rail during amplification (i.e. clipping). Thus, the output signal of a typical inverter might be characterized as a clipped sine wave. *This particular nonlinearity characteristic of the inverter further provides opportunities for phase*

noise to be added to the output signal. (emphasis added) (col. 23, lines 1- 12)

* * *

Thus, in the present invention, phase noise is minimized in the nonlinear buffer amplifiers 1352, 1354, and 1556 by amplifying the differential signal provided by the crystal oscillator circuit through the *linear amplifier* 720 in order to increase the amplitude, and thus the slew rate, of the signal prior to its conversion a square wave. *Phase noise resulting from zero crossing of the nonlinear buffer amplifiers is thereby minimized.* (emphasis added) (col. 23, lines 15-22).

* * *

Additionally, *the use of linear buffer amplifiers followed by non-linear amplification* in a reference oscillator circuit is a unique improvement over the prior art in reducing phase noise. (emphasis added) (col. 26, lines 1-4).

In view of the foregoing amendment and remarks, allowance of this patent application is respectfully requested.

If necessary to effect a timely response, this paper should be considered as a petition for an Extension of Time sufficient to effect a timely response. Please charge any such fee or any deficiency in fees, or credit any overpayment of fees, to Deposit Account No. 05-1323 (Docket 100630.53029US).

Respectfully submitted,

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CERTIFICATE OF MAILING/TRANSMISSION (37 CFR 1.8A)

I hereby certify that this correspondence is, on the date shown below, being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.

August 18, 2004
Date

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Laura R. Dixon